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| 10/693,462 | 10/27/2003 | Alexander Krymski | M4065.0979/P979 | 2941 |

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| EXAMINER | |
|---|---|
| NGUYEN, LINH V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/693,462 | KRYMSKI, ALEXANDER | |
| | Examiner | Art Unit | |
| | Linh V Nguyen | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *35* is/are withdrawn from consideration.

5)☒ Claim(s) *1-30* is/are allowed.

6)☒ Claim(s) *31,32,34,36,37 and 39-47* is/are rejected.

7)☐ Claim(s) *33 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/03*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *09/22/04* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application No. 10/734,268 filed on 10/27/03. Claims 1 – 47 are pending on this application.

### *Election/Restrictions*

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1 - 34, 36 - 47 drawn to Analog-to-Digital converter system, classified in class 341, and subclass 155.

II. Claim 35, drawn to reference voltage generator with switching capacitor network, classified in class 341, and subclass 172.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. Chris Chow on 08/10/04, a provisional election was made without traverse to prosecute the invention of Group I, which includes claims 1 – 34, and 36 - 45. Affirmation of this election must be made by applicant in replying to this Office action. Claim 35 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

### *Specification*

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Objections*

6. Claims 46 and 47 are objected to because of the following informalities:

Claim 46 is a duplication of claim 41, and claim 47 is a duplication of claim 43, because each of the above claims is directly depending on claim 40.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 31, 32, 34, 36, 37, 39, 40 – 43, 46 and 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Yakovlev U.S. Patent No. 6,670,904.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 31, Fig. 2 and 3 of Yakovlev disclose a method for converting an analog signal to a digital word (Col. 3 lines 57 – 58), comprising: measuring a magnitude of said analog signal (Col. 3 lines 64 – 65); if said magnitude (Fig. 3 [Vin]) is not greater than a first threshold (Fig. 3 [Vc]; between the fifth and sixth vertical dot-lines of Fig. 3; See Col. 4 lines 48 – 49), mapping said magnitude to a digital word (Fig. 3 [Output Code D5....D0]; See Col. 4 lines 51 – 52) in accordance with a first transfer function (Fig. 3 [Vcmp] from low to high; See Col. 4 lines 49 – 52); and if said magnitude (Fig. 3 [Vin]) is at least equal to said first threshold (Fig. 3 [Vc]; See Col. 4 line 24 - 25), mapping said magnitude to the digital word (Fig. 3 [D11....D6] Col. 4 lines 26 – 28) in accordance with a second transfer function (Fig. 3 [Vcmp] from high to low; Col. 4 lines 25 – 26).

Regarding claim 32, wherein said first transfer function (Fig. 3 [Vcmp] from low to high) maps each magnitude (Fig. 3[Vin]) below said first threshold (Fig. 3 [Vc]) to a corresponding reference signal (Fig.3 [Vfine]) in a linear manner (Fig. 3 disclosing the mapping Vin magnitude below threshold Vc in a straight line graph; wherein straight line graph is a definition of linearity. See Webster Dictionary).

Regarding to claim 34, wherein said second transfer function (Fig. 3 [Vcmp] from high to low) maps each magnitude at least equal to said first threshold (Fig. 3 [Vc]; Col.

4 lines 24 – 25) to corresponding reference signals (Vcoarse, Vfine) in a logarithmic manner (Col. 5 lines 12 – 15 disclosing logarithm manner [$2^6$]).

Regarding claim 36, Fig. 2 and 3 of Yakovlev disclose a method for operating an imaging system (col. 1 lines 5 – 6), comprising: receiving an analog pixel signal (Fig. 2 [Vin] from a pixel (Col. 3 lines 35 – 37); converting said analog pixel signal into a digital word (Col. 3 lines 35 – 37), wherein said converting comprises: measuring a magnitude of said analog signal (Col. 3 lines 64 – 65); if said magnitude is not greater than a first threshold (Fig. 3 [Vc]; between the fifth and sixth vertical dot-lines of Fig. 3; See Col. 4 lines 48 – 49), mapping said magnitude to a digital word (Fig. 3 [Output Code D5....D0]; See Col. 4 lines 51 – 52) in accordance with a first transfer function (Fig. 3 [Vcmp] from low to high; See Col. 4 lines 49 – 52); and if said magnitude (Fig. 3 [Vin]) is at least equal to said first threshold (Fig. 3 [Vc]; See Col. 4 line 24 - 25), mapping said magnitude to the digital word (Fig. 3 [D11....D6] Col. 4 lines 26 – 28) in accordance with a second transfer function (Fig. 3 [Vcmp] from high to low; Col. 4 lines 25 – 26).

Regarding claim 37, wherein said first transfer function (Fig. 3 [Vcmp] from low to high) maps each magnitude (Fig. 3 [Vin]) below said first threshold (Fig. 3 [Vc]) to a corresponding reference signal (Fig. 3 [Vfine]) in a linear manner (Fig. 3 disclosing the mapping Vin magnitude below threshold Vc in a straight line graph; wherein straight line graph is a definition of linearity. See Webster Dictionary).

Regarding claim 39, wherein said second transfer function (Fig. 3 [Vcmp] from high to low) maps each magnitude at least equal to said first threshold (Fig. 3 [Vc]; Col.

4 lines 24 – 25) to corresponding reference signals (Vcoarse, Vfine) in a logarithmic manner (Col. 5 lines 12 – 15 disclosing logarithm manner [$2^6$]).

Regarding claim 40, Fig. 1 of Yakovlev discloses an imaging system, comprising: a pixel array (200); an analog to digital converter circuit (Fig. 2, Col. 2 lines 65 – 67) that receives analog signals (Fig. 2 [Vin]) from the pixel array and converts the analog signals to digital signals (Col. 3 lines 35 – 37); wherein said AD converter circuit converts with a variable level of quantization (Col. 4 lines 8 – 12, discloses AD converter having variable level quantization of Most Significant Bits for coarse level and Least Significant Bits for fine level quantization).

Regarding to claim 41, wherein said AD converter circuit comprises: a variable quantization AD converter (Col. 4 lines 8 – 12, discloses AD converter having variable level quantization of Most Significant Bits for coarse level and Least Significant Bits for fine level quantization).

Regarding claim 42, wherein said variable quantization AD converter is a ramp type AD converter (Col. 2 line 39).

Regarding claim 43, wherein said AD converter circuit comprises: a linear AD converter (Fig. 2 disclosing AD converter, and Fig. 3 disclosing the mapping Vin magnitude below and above threshold Vc in a straight line graph; wherein straight line graph is a definition of linearity. See Webster Dictionary); and a processing circuit (Fig. 5) that remaps values output (Fig. 5 [Vcmp]) by said linear AD converter (Fig. 5 [FROM ADC]; See Col. 6 lines 25 – 34).

Regarding to claim 46, wherein said AD converter circuit comprises: a variable quantization AD converter (Col. 4 lines 8 – 12, discloses AD converter having variable level quantization of Most Significant Bits for coarse level and Least Significant Bits for fine level quantization).

Regarding claim 47, wherein said AD converter circuit comprises: a linear AD converter (Fig. 2 disclosing AD converter, and Fig. 3 disclosing the mapping Vin magnitude below and above threshold Vc in a straight line graph; wherein straight line graph is a definition of linearity. See Webster Dictionary); and a processing circuit (Fig. 5) that remaps values output (Fig. 5 [Vcmp]) by said linear AD converter (Fig. 5 [FROM ADC]; See Col. 6 lines 25 – 34).

9. Claim 45 is rejected under 35 U.S.C. 102(b) as being anticipated by Gowda et al. U.S. Patent No. 5,920,274.

Fig. 3 of Gowda et al. disclose an integrated circuit (Col. 1 lines 16 – 18), comprising: a pixel array (IMAGE SENSOR ARRAY), disposed on said integrated circuit (Fig. 3); and an analog to digital (42, See Col. 5 lines 26 - 27) converter circuit, disposed on said integrated circuit (Fig. 3), wherein said analog to digital converter circuit (42) receives analog signals (15) from the pixel array (IMAGE SENSOR ARRAY) and converts the analog signals (15) to digital signals (45) with a variable level of quantization (VREF, See Col. 6 lines 24 – 25).

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yakovlev as applied to claim 43 above, and further in view of Gowda et al. as applied to claim 45 above.

Yakovlev as applied to claim 43 above disclosing a processing circuit (Fig. 5) that remaps values output (output (Fig. 5 [Vcmp]) from AD converter (Fig. 5 [FROM ADC]; See Col. 6 lines 25 – 34). However Yakovlev fails to disclose wherein said processing circuit remaps values by consulting a mapping table.

Fig. 5 of Gowda et al. discloses a processing circuit (59) that remaps values output (55) from AD converter (42, Col. 6 lines 43 – 44) by consulting a mapping table (Col. 6 lines 61 – 65).

Yakovlev and Gowda et al. are common subject matter for image sensor with Analog-to-Digital converter. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated mapping table of process circuit taught by Gowda et al. into mapping process circuit of Yakovlev for the purpose of providing maps each input code to a corresponding output code

according to mapping function stored in a look-up table (Gowda et al., Col. 6 lines 62 – 65).

***Allowable Subject Matter***

12. Claims 33 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior arts fail to teach or suggest a method of transfer function wherein said second transfer function maps a set of non-sequential and increasing magnitudes each at least equal to said first threshold to corresponding reference signals in a linear manner.

13. Claims 1 – 30 are allowed. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 1, 11, and 21, in addition to other elements in the respective claim, the prior art fails to teach or suggest a control circuit for determining the digital word corresponding to the input signal by repeatedly: comparing the magnitude of the input signal with the magnitude of a most recently generated reference voltage of said sequence, incrementing said counter, and causing said ramp generator to generate a new one of said sequence until the magnitude of the most recently generated reference voltage of said sequence exceeds the magnitude of said input signal.

***Cited References***

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references relate to Analog to Digital converter for image sensor system.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

09/22/2004

Linh Van Nguyen

Art Unit 2819